

4500 GENIE* BUS EXTENDER/BUS EXTENDER SWITCH MAINTENANCE

AXBE/AXES-M
7/14/78

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4500 GENIE*

BUS EXTENDER/BUS EXTENDER SWITCH MAINTENANCE

1. INTRODUCTION

This publication provides maintenance-related information for the Bus Extender and Bus Extender Switch modules used on 4500 process computer systems.

2. PRECAUTIONS

The Bus Extender and Bus Extender Switch boards contain only logic level voltages, but to avoid damage to the logic, power must always be removed prior to removal or replacement of the boards.

Do not change any of the switch settings at the PWA front edge without first considering the possible effect on an on-line computer system. Change the switches only when necessary and after any concerned personnel are notified.

3. OPTIONS

Two models are available: Model AXBE, Bus Extender and Model AXES, Bus Extender Switch. Both models can be option pinned as follows (see Fig. 1):

- 4400/4500 Operation
- Bus Extender Only/Bus Extender Switch Operation
- De-select/Don't De-select Operation (under computer control)

Both models require priority and address switch selections. See 9. and Fig. 1 for option pinning and switch locations.

4. REFERENCE DOCUMENTS

ACPU1GBC-T	GENIE Bus Theory
ACPU1GBC-M	GENIE Bus Maintenance
AXBE/AXES-T	Bus Extender/Bus Extender Switch Theory
4500GI-M	4500 General Maintenance Information
	Miscellaneous Test Programs for the Devices on the Slave Bus
ATPG-I	ATPG Programs - How to Load Them, Run Them, and Use Them

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5. COMPONENT LOCATIONS

The Bus Extenders and/or Bus Extender Switches are located on the Master Bus in the CPU cabinet. The Master Bus consists of the I/O Chassis and their card slots which are driven directly from the GBC. The Bus Extender is marked "AXBE11". The Extender Switch is marked "AXES11".

6. TEST EQUIPMENT

The general test equipment related to maintenance for the computer system is listed in Section 6.1 of the 4500 Process Computer General Maintenance Information publication, 4500GI-M.

7. PREVENTIVE MAINTENANCE

Preventive maintenance is not required for these modules.

8. PERFORMANCE TESTS

Performance of the Bus Extender and/or Bus Extender Switch can be verified via the use of various Test Programs for the devices on the Slave Bus.

Instructions for operation of these Test Programs are provided with the punched cards or tape, plus, reference to publication ATPG-I may prove useful.

9. ASSEMBLY AND DISASSEMBLY

Assembly and disassembly consists only of removal and reinsertion of PWB's. Note that when replacing one of these PWB's with a new one requires the setting of the address and priority selection switches plus the insertion of option pins.

9.1 Address and Priority Selection

Switch packs S4 and S5 provide for address and priority selection as shown on Fig. 1. Consult system documentation for specific switch settings for individual PWB's.

9.2 Option Pin Placement

Option pins should be placed on the PWB in the positions specified for each individual PWB per the System's documentation. Option Pin Locations are shown on Fig. 1.

10. ADJUSTMENTS

There are no adjustments related to the Bus Extender, Model AXBE.

There is one adjustment on the Bus Extender Switch, Model AXES. This adjustment (R24) is used to adjust the +5 Vdc to +5 V \pm 5% as measured between the PV5 Plane and dc common. See Fig. 1 for location of R24.

11. TROUBLESHOOTING

Because the Bus Extenders and Bus Extender Switches are intrinsic components of the overall GENIE Bus, troubleshooting of them individually is impractical. Therefore, the troubleshooting section in the 4500 GENIE Bus Maintenance publication, ACPUIGBC-M, provides the informa-

tion necessary to isolate faults to the Extender/Switch PWB or to the Slave Bus level.

12. PARTS

The Bus Extender and Bus Extender Switch are considered non-repairable in the field, therefore, the PWA's are the only replaceable parts.

Bus Extender -

Model AXBE - PWA part no. 4DP3AAXBE11.

Bus Extender Switch -

Model AXES - PWA part no. 4DP3AAXES11.

Cable -

Multi-Bus Extender Cable - 51300202

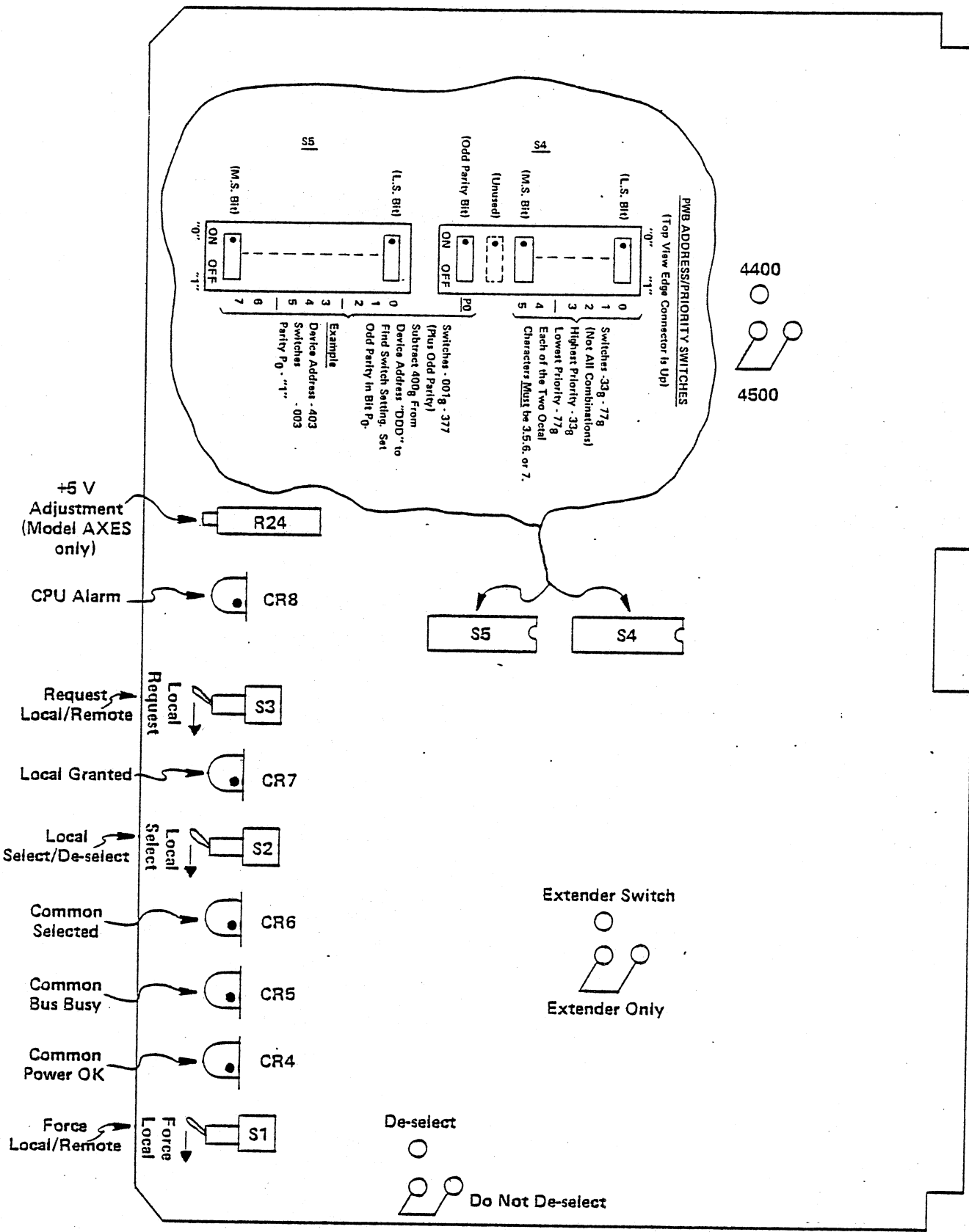


Fig. 1 Switch/Pin Options

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4500 GENIE* BUS EXTERNAL "DEVICE" API MODULE MAINTENANCE

AIIE-M
3/1/78

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4500 GENIE* BUS EXTERNAL "DEVICE" API MODULE MAINTENANCE

1. INTRODUCTION

This publication provides Maintenance related information for the model AIIE External "Device" API Module used on the 4500 process computer systems. This External "Device" API Module will be referred to simply as an interrupt module throughout the remaining text of this publication.

2. PRECAUTIONS

The interrupt module board contains only logic level voltages, but to avoid damage to the logic, power must always be removed prior to removal or replacement of the board.

3. OPTIONS

Only one board model is available, Model AIIE, but, this board does contain switch selection options for address, priority, and external input edge selection. It also provides pinning options for selection of: interface type, input filter/delay time, interrupt inhibit/non-inhibit type, TIM/TOM/Event, and ECHO/STOR setting of the interrupts. These switch selections and pinning options are discussed in the following paragraphs.

3.1 Address and Priority Selection

Switch packs S1 and S2 provide for address and priority selection as shown on Fig. 1. For location of switches on board, see Fig. 2. Consult system documentation for specific switch settings for individual boards.

3.2 External Input Edge Selection

This switch pack allows the PR1 (Non-inhibit) or PR2 (Inhibit) interrupt signal to be generated from either the positive edge or the negative edge, per switch setting, of the individual external interrupt signal per Fig. 3. The eight external lines are marked "A" through "H".

3.3 Option Pinning

Option pin locations are shown on Fig. 2. Option pinning information and a simplified circuit drawing of one of the external device interrupt inputs is provided on Fig. 4. Fig. 4 also provides information on the input filter/delay timing pinning options plus additional information about the PED/NED switch (S3) selection.

Option pins also provide the assignment of "inhibit" or "non-inhibit" status to each interrupt. In addition, option pins are used to designate whether interrupts "A", "C", "E", and "G" are of a TIM, TOM or EVENT type and other option pins are used to determine whether interrupts "B", "D", "F", and "H" may be SET by an ECHO signal from the GBC. These option pins are shown on Fig. 2.

3.4 Interrupt Interface Connector Assembly

The external interrupt inputs are connected to the interrupt module via an assembly which connects onto the I/O modules backpanel's "B" connector pins, those associated with the card slot where the interrupt module is located. This assembly consists of a connector, printed circuit card, and a barrier terminal strip. The external device's interrupt inputs are connected to the barrier terminal strip as indicated on Table 1.

4. REFERENCE DOCUMENTS

ACPU1GBC-T	GENIE Bus Theory
ACPU1GBC-M	GENIE Bus Maintenance
4500GI-M	4500 General Maintenance Information
51191010	External API Module Test Program
ATPG-I	ATPG Programs - How to Load Them, Run Them, and Use Them
AIIE-T	4500 GENIE External "Device" API Module Theory

5. COMPONENT LOCATIONS

The interrupt module will be located on either the GENIE master bus or on one of the GENIE slave busses. This module is identified via the following identification marked on the board: PX4000IPEA1. The connection assembly is located on the I/O modules "B" connector pins per the slot where the interrupt module board is located.

6. TEST EQUIPMENT

The general test equipment related to maintenance for the computer system is listed in Section 6.1 of the 4500 Process Computer General Maintenance Information publication, 4500GI-M.

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7. PREVENTIVE MAINTENANCE

Preventive maintenance is not required for this module.

8. PERFORMANCE TESTS

Performance of the 4500 GENIE Bus External "Device" API Module is verified via the use of its Test Program, number 51191010.

Instructions for operating this test program are provided with the punched cards or tape. Reference to publication ATPG-I may prove useful.

9. ASSEMBLY AND DISASSEMBLY

Assembly and disassembly consists only of removal and reinsertion of PWBs. Note that when replacing one of these PWBs with a new one, it is required that the address and priority switches be properly selected plus all option pins must be correctly inserted. See Section 3 (OPTIONS) for switch and option pinning information.

10. ADJUSTMENTS

There are no adjustments related to this module.

11. TROUBLESHOOTING

Because this module, when implemented, becomes an intrinsic component of the overall GENIE Bus, troubleshooting if done individually is impractical. Therefore, the troubleshooting section in the 4500 GENIE Bus Maintenance publication, ACPUI1GBC-M, in conjunction with this module's test program, provides the information necessary to isolate most faults to the board level.

12. PARTS

The interrupt module functionally consists of the PX4000IPEA1 PWB and an Interrupt Interface Connector Assembly.

4500 GENIE Bus External "Device" API Module - Model AIIE - PWB part no. PX4000IPEA1.

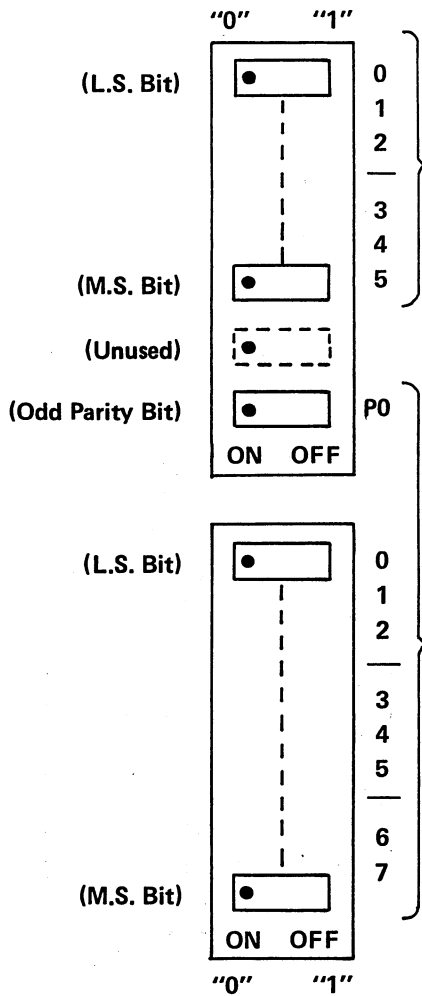
Interrupt Interface Connector Assembly - Assembly part no. 51103184-100.

Parts of Assembly:

- Printed Circuit Card - 51103126-100
- Modified Connector - 51100202-100
- Barrier Terminal Strip - 43C950098P16

PWB ADDRESS/PRIORITY SWITCHES

(Top View Edge Connector is Up)



Bus Priority Assignment

LOC: H-7/8

Relative priority within a section of the I/O Bus (1 of 16) is determined by switches as shown below:

Device Address (& Parity)

LOC: H-6/7

The Eight-Line Int. PWB utilizes four device addresses, (two interrupts per address) with the starting address of four sequential addresses set in the switches. Address range: 000_8 to 377_8 . Starting address must have least significant octal character = 0_8 or 4_8 ($XX0_8$ or $XX4_8$). Set "Parity" for odd parity.

PRIORITY	(H) 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	(L) 16
SW. CONFIG. (8)	33	35	36	37	53	55	56	57	53	65	66	67	73	75	76	77

Fig. 1 Address/Priority Selection

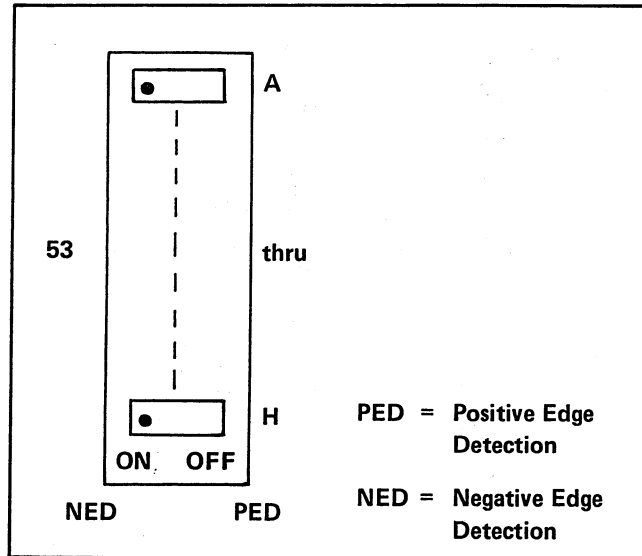


Fig. 3 External Input Edge Selection Switch

CONNECTOR ASSEMBLY		INTERRUPT MODULE	
Barrier Strip No.	Connector Pin No.	Interrupt Module Pin No.	Circuit Designation
1	30	B30	
2	80	B31	A
3	31	B31	
4	81	B81	B
5	32	B32	
6	82	B82	C
7	33	B33	
8	83	B83	D
9	34	B34	
10	84	B84	E
11	35	B35	
12	85	B85	F
13	36	B36	
14	86	B86	G
15	37	B37	
16	87	B87	H

Table 1 External Device Interrupt Connections

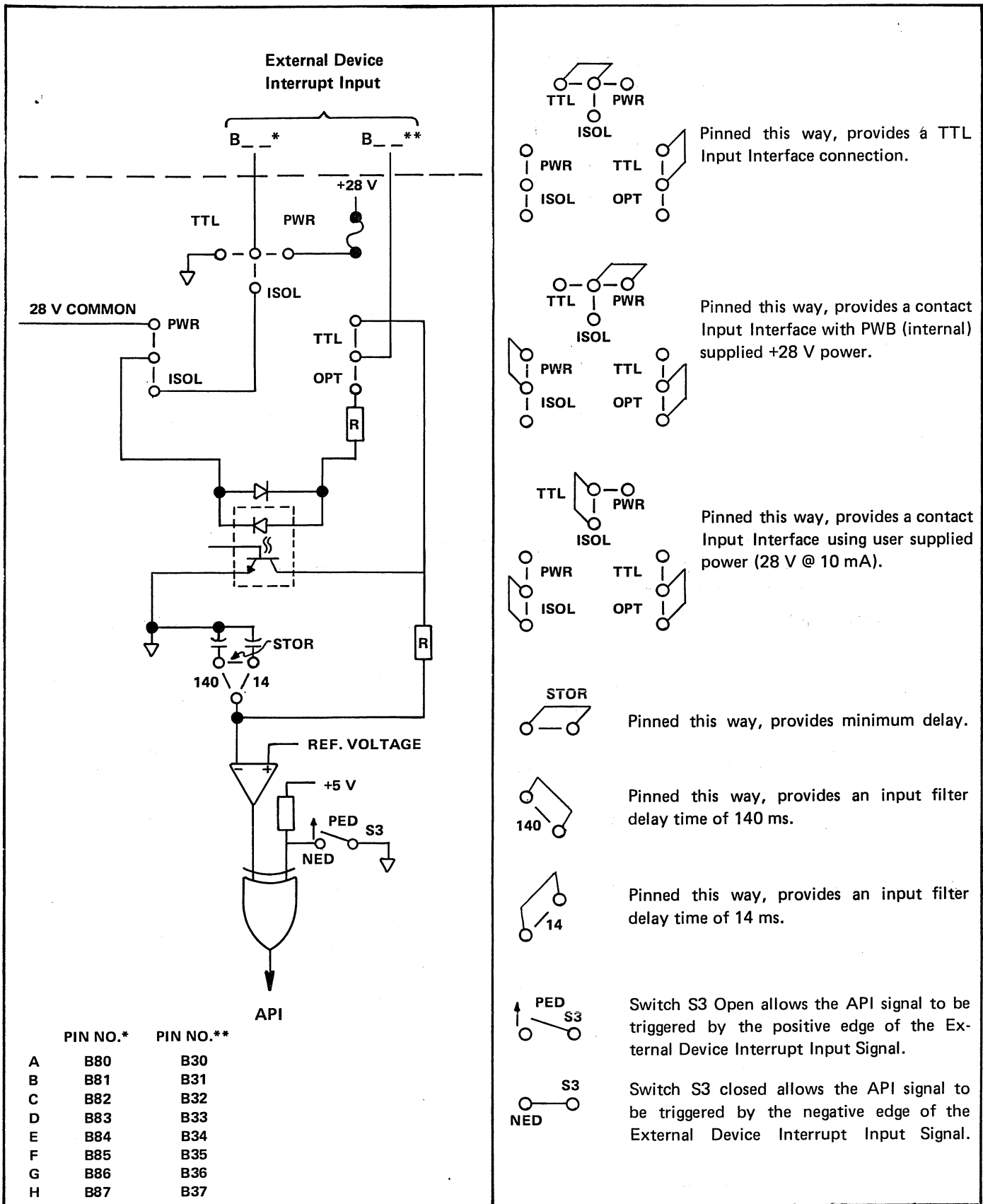


Fig. 4 External Device Interrupt Input Circuit

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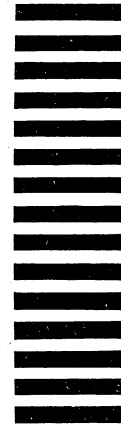
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